Journal of the Ceramic Society of Japan 117 [9] 1032-1034 2009 **Paper**

$(Bi,La)_4Ti_3O_{12}$ as a ferroelectric layer and $SrTa_2O_6$ as a buffer layer for metal-ferroelectric-metal-insulator-semiconductor field-effect transistor

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The metal-ferroelectric-metal-insulator-semiconductor field-effect transistor (MFMIS–FET) using the $(Bi,La)_4Ti_3O_{12}$ (BLT) as a ferroelectric and $SrTa_2O_6$ (STA) as a buffer layer is prepared. The Au/STA/Si structure shows about 1 nF/cm^2 of the accumulation capacitance value which is equivalent to about 6.2 nm of SiO_2. The leakage current density is lower than 10^7 A/cm^2 under 5 V. The remanent polarization of the 420 nm-thick BLT film was 35.2 μC/cm^2 at 450 kV/cm. The MFMIS–FET was fabricated with different area ratio (A_I/A_F) from 1 to 8. From the drain current–gate voltage characteristics at the drain voltage of 0.2 V, the memory window is only 0.5 V for the device with A_I/A_F = 1 but it is increased to 1.8 V as the A_I/A_F is increased to 8. For the A_I/A_F ratio of 8, the "on" state of the drain current of 1.12×10^{-5} A rapidly drops after 10^5 s to 2×10^{-6} A and the "off" state current increase from 10^{-7} A to 10^{-6} A after 10^5 s. The on/off current ratio decrease from 3×10^2 to 8.

Key-words : MFMIS structure, $(Bi,La)_4Ti_3O_{12}$, $SrTa_2O_6$, FeRAM, Retention time

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1. Introduction

Ferroelectric random access memory (FeRAM) is one of the most promising candidates for this new type of memory device and thus research and development of FeRAM are being conducted actively in many semiconductor companies.[1)]

Initially, for FeRAM, the metal-ferroelectric-semiconductor structure (MFS) has been suggested. However, MFS structure shows serious problems such as chemical reactions and the interdiffusion between the Si and ferroelectric films. In view of this, metal-ferroelectric-insulator-semiconductor structures (MFIS) are suggested where an insulator layer is inserted between the ferroelectric and silicon substrate. However, the insulator layer could be the structural factor that reduces the retention time to become short in MFIS structures.[2),3)]

To overcome the retention problem, metal-ferroelectric-metal-insulator-semiconductor field-effect transistor (MFMIS–FET) using $Pb(Zr,Ti)O_3$ (PZT) and silicon dioxide (SiO_2) as a ferroelectric and a gate insulator, respectively.[4)] In this structure, the excellent interface properties of SiO_2/Si are available. However, it becomes difficult to apply sufficient voltage to the PZT film because the dielectric constant of PZT films is much higher than SiO_2. In consideration of the above reasons, the high-k dielectrics as insulator including $LaAlO_3$, Al_2O_3, $LaZrO_x$ and HfO_2 are studied. These high-k materials posses dielectric constant in the range from 10 to 50 and have low leakage current and good interface characteristics on Si.[5–8)]

In this work, we evaluated the characterization of MFMIS structures using $SrTa_2O_6$ film that has much higher dielectric constant (40–120) than SiO_2 as an insulator layer and $(Bi,La)_4Ti_3O_{12}$ film as a ferroelectric layer.

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2. Experiment

The SiO_2 field as a diffusion barrier was formed by the thermal oxidation process. After definition of the source and drain region by photolithography, a phosphosilicate glass (PSG) thin film was spin-coated to use a doping source of phosphorous. The thermal diffusion was performed at 1050°C for 45 s via rapid thermal annealing (RTA). The PSG and SiO_2 on the Si wafer were removed by soaking into a buffered oxide etchant.

The STA sol–gel solution was spin-coated on the source and drain dopped Si wafer at 5000 rpm for 25 s. The coated film was dried at 150°C on a hot-plate to remove the residue solvent. To improve the crystalline of the STA film, the STA/Si structure was annealed in the RTA at 900°C for 3 m in ambient O_2.

For the intermediate electrode, the Pt was deposited on the STA/Si by an ion sputter and the patterns were defined by wet etching process.

The BLT solution, with a stoichiometric composition of $Bi_{3.25}La_{0.75}Ti_3O_{12}$, was spin-coated on the Pt/STA/Si structure at 3000 rpm for 25 s. Then, it was dried at 250°C for 10 m on a hot-plate to evaporate the solvent. To obtain the desired thickness, these coating and drying procedures were repeated several times. The structure was crystallized at 750°C for 30 m in ambient O_2. The Au electrode was thermally evaporated on the sample surface to investigate electrical properties of the STA/Si and BLT/Pt/STA/Si structures.

The electrical properties of the Au/STA/Si and the Au/BLT/Pt/STA/Si structure were characterized by using the HP 4280A capacitance-meter, Precision LC parameter analyzer and Agilent 4155C precision semiconductor parameter analyzer.

3. Results and discussion

In **Fig. 1**, the capacitance-voltage (C–V) curve of Au/STA/Si structure for a bias sweeping range of ± 4 V is shown. A large

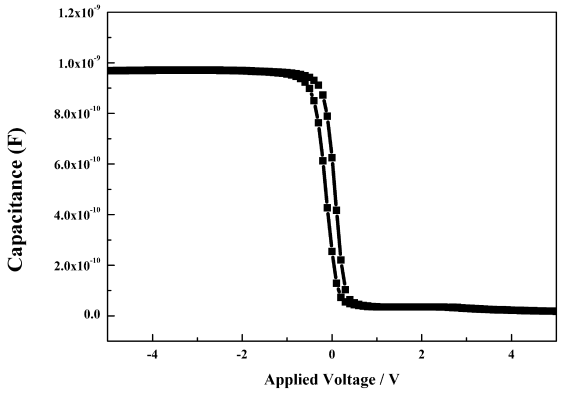

Fig. 1. Capacitance-voltage characteristic of Au/STA/Si structure. The capacitance of the STA is 1 nF/cm^2 at –4 V, which corresponds the equivalent oxide thickness of 6.2 nm.

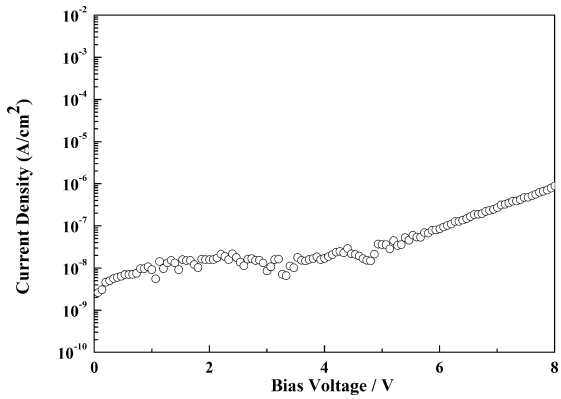

Fig. 2. Current density-bias voltage curve of the Au/STA/Si structure. The leakage current density was smaller than 10^{-7} A/cm^2 under 5 V.

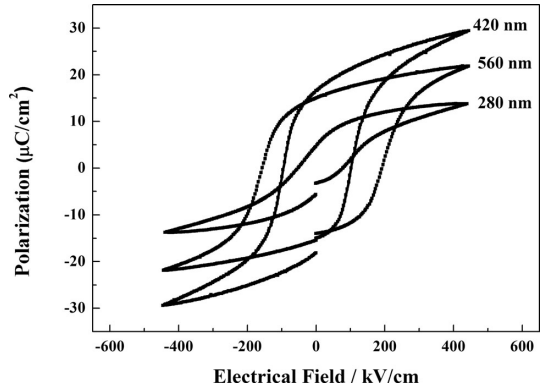

Fig. 3. Polarization-electric field hysteresis curves of 280 nm-, 420 nm- and 560 nm-thick BLT film.

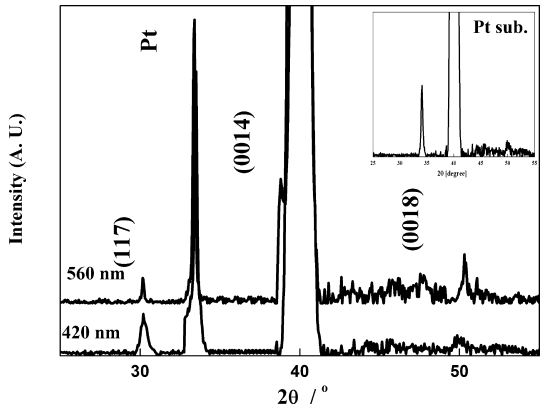

Fig. 4. XRD patterns of the 420 nm- and 560 nm-thick BLT film.

capacitance for an insulator is required to distribute enough bias voltage to the ferroelectric layer in MFMIS structure. The Au/STA/Si structure shows about 1 nF/cm^2 of the accumulation capacitance value which is equivalent to about 6.2 nm of SiO_2. The heat treatments to crystallize the structure may have reduced the total dielectric constant of the interfacial oxide layer since it has been reported that a thin silicon dioxide layer exists between the STA and Si substrates even if the STA film is annealed at temperatures as low as 700°C.[9)]

The current density-bias voltage characteristic of the Au/STA/Si structure measured at room temperature is shown in **Fig. 2**. The measured leakage current density was found to be less than 10^{-7} A/cm^2 under 5 V, which is much smaller than the leakage current density (~10^{-6} A/cm^2) expected for the SiO_2 film.

Figure 3 shows the polarization-electric field (*P–E*) hysteresis loops of various BLT films with different thickness. The remanent polarization ($2P_r$) of the 280 nm, 420 nm and 560 nm-thick BLT thin films are 10.05, 35.2, 29.4 μC/cm^2, respectively, when they are subject to a field of 450 kV/cm. Although all the films exhibited well-defined *P–E* loops, the maximum of $2P_r$ corresponds to the 420 nm-thick BLT film and not the thickest 560 nm one. Besides, the thicker film's coercive field is higher than for the thin one.

From the XRD pattern of the BLT films in **Fig. 4**, the reason which observed in Fig. 3 came out. Lee et al., have reported the ferroelectric properties of epitaxial BLT thin films grown with (001) and (118) orientation. Their results have shown that remanent polarization measured along the *a*-axis is about two times that along the *b*-axis. This trend agrees with our results in that the (001)-oriented BLT thin film remanent polarization is lower than that of (117)-oriented films.[10)] For the film annealed at 750°C, diffraction peaks that corresponded to (117), (0014) and (0018) reflections were observed. Among these peaks, the remark peak near 30° indicates that the BLT film has a ferroelectric property and the intensity of the 420 nm film is bigger than 560 nm. Moreover, the 560 nm film indicated the (001)-oriented diffractions such as (0018), (0014) even though it didn't show in the patterns of the 420 nm film. So, from this pattern, the both BLT films, in this work, were defined well through highly *c*-axis oriented preferential growth with a fraction of (117) but the thicker film easier to be formed (001)-orientation that has lower polarization value.

The drain current (I_D)-gate voltage(V_G) characteristics of Au/BLT/Pt/STA/Si MFMIS–FET at V_D of 0.2 V changed with the area ratio (A_I/A_F) is shown in **Fig. 5**. The counterclockwise hysteresis loop due to the ferroelectric nature of the BLT film can also be seen as indicated by the arrows. The tendency of the on/off current ratio and the memory window with different A_I/A_F were summarized in **Fig. 6**. The gate voltage sweep is ± 7 V and the A_I/A_F is varied from 1 to 8. In case of the area ratio of 1, it looks like the metal-ferroelectric-insulator-semiconductor (MFIS) structure, the threshold voltage shift or the memory window is only 0.5 V for the device with A_I/A_F = 1, which indicates that only one of the minor *P–E* loops is used because there was not enough bias applied to the BLT film because of the relatively low capacitance of the STA film. On the other hand, when the A_I/A_F is as larger as 8, the memory window is almost 1.8 V,

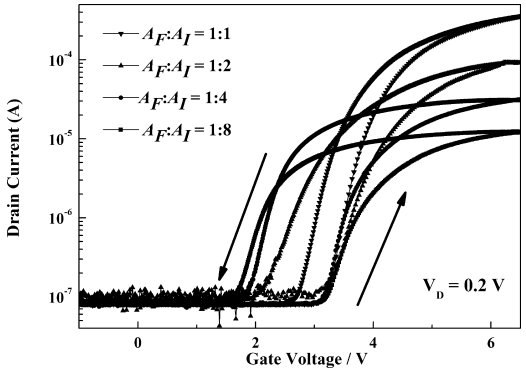

Fig. 5. Drain current-gate voltage characteristics of MFMIS–FET with different area ratio. The counterclockwise hysteresis loops due to the ferroelectric nature of the BLT film are observed as indicated by arrows.

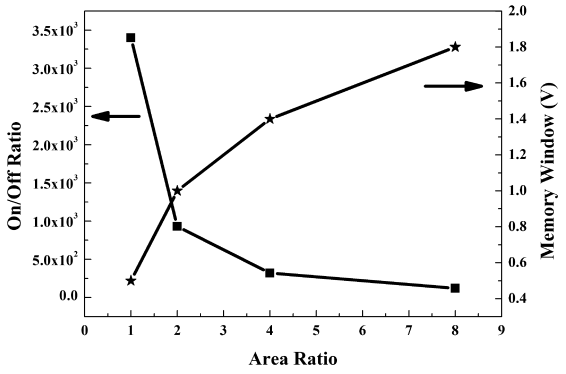

Fig. 6. Tendency of the on/off current ratio and the memory window with different area ratio (A_F/A_I). As the A_F/A_I increased, the on/off current ratio decreased but the memory window increased.

which shows the saturated *P–E* hysteresis loop is being effectively used in the devices with such area ratios.

Figure 7 shows the "on" and "off" state drain current of MFMIS–FET with area ratio of 8 as a function of the time. In order to measure the time, firstly, a 7 V programming pulse is applied to write information and then, the gate voltage is kept at 3 V during a certain retention time and measuring while keeping the drain voltage at 0.2 V. The on state of the drain current starts around 1.12×10^{-5} A and rapidly drops to 2×10^{-6} A and the off state current increase from 10^{-7} A to 10^{-6} A after 10^5 s. The on/off current ratio decrease from 3×10^2 to 8.

4. Conclusion

Using the BLT ferroelectric films as a ferroelectric layer and the STA as an insulator, the MFMIS–FET has been investigated. The well defined sol–gel derived STA thin film and the BLT films have been prepared with optimum conditions for each layer.

The equivalent oxide thickness of the STA thin film annealed at 900°C is about 5.2 nm and the leakage current density at an applied voltage of 5 V was lower than 10^7 A/cm^2.

The BLT film thickness of 420 nm has been shown to have the best behavior with a *2Pr* being 35.2 μC/cm^2 when the applied field is 450 kV/cm.

The Au/BLT/Pt/STA/Si structure with different area ratios ranging from 1 to 8 have been fabricated. From the drain current–gate voltage characteristics at the drain voltage of 0.2 V, the memory window is only 0.5 V for the device with the A_I/A_F ratio

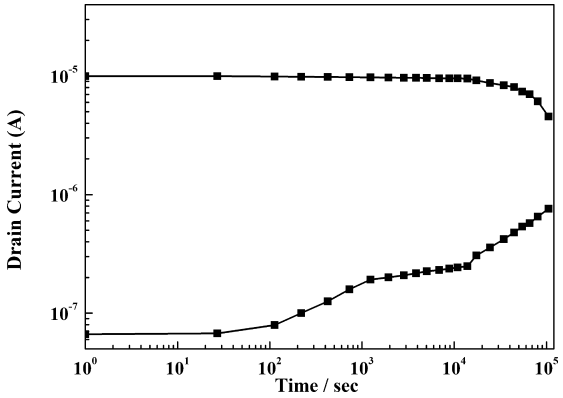

Fig. 7. Retention time characteristic of the MFMIS structure for A_I/A_F of 8.

being equal to unit but this increase to 1.8 V when A_I/A_F = 8. Moreover, the on/off current ratio is decreased from 5×10^3 to 2×10^2. Finally, the data retention characteristic of writing the data has been examined and results indicate that the data retention characteristics can be improved by increasing the area ratio. The data retention time for an area ratio of 1 was only few m. However, for an area ratio of 8, the drain current of 1.12×10^{-5} A rapidly drops after 10^5 s to 2×10^{-6} A. It's relatively short retention time for FeRAM because the I_D of the on-state is too large value of 10^{-5} A. The large drain current increased the possibility that the carrier built from channel, pass through the gate stack. It makes the polarization of the BLT reduced, abruptly. The large drain current, fortunately, can be reduced by engineering the transistor to improve the retention time.

From these results, the combination of BLT and STA films could offer useful options for nonvolatile ferroelectric memory device with controlling the area ratio.

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