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Characteristics of Au/SBT/LZO/Si MFIS structure for ferroelectric-gate field-effect transistors

Jong-Hyun IM and Byung-Eun PARK†

School of Electrical and Computer Engineering, University of Seoul, 90 Jeonnong-dong, Dongdaemun-gu, Seoul 130−743 Korea

Non-volatile memories using ferroelectric-gate field-effect transistors (Fe–FETs) with metal/ferroelectric/semiconductor gate stack (MFS–FETs) have superior advantages such as non-destructive read operation and high density. However, the interfacial reactions between ferroelectric materials and Si substrates make it difficult to obtain good electrical properties of MFS–FETs. As an alternative solution, Fe–FETs with a metal/ferroelectric/insulator/insulator/semiconductor gate stack (MFIS–FETs) have been proposed. We prepared $SrBi_2Ta_2O_9$ (SBT) film as a ferroelectric layer and $LaZrO_x$ (LZO) film as the insulating buffer layer, and then fabricated the n-channel Fe–FETs with the Au/SBT/LZO/Si structure. The thickness of the LZO buffer layer and SBT film deposited by a sol–gel method were about 35 nm and 450 nm, respectively. From the electrical properties of the LZO film on Si, no hysteresis was observed in the *C–V* curve and the leakage current density was about 1.4×10^{-7} A/cm^2 at 5 V. SBT film on the LZO/Si structure was crystallized in a polycrystalline phase with a highly preferred (115) orientation. The *C–V* characteristics of Au/SBT/LZO/Si structure showed a clockwise hysteresis loop and the memory window width increased as the bias voltage increased. The fabricated Fe–FETs showed typical n-channel MFIS–FETs *C–V* characteristics and the current on/off ratio was about 10^3. Also, the memory window width was about 0.7 V.

Key-words : MFIS–FET, SBT, Buffer layer, LZO, Ferroelectric

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1. Introduction

Recently, there has been a growing interest in non-volatile ferroelectric random access memory (NVFRAM) devices. Non-volatile memories using ferroelectric capacitors have been extensively researched, which utilize basically destructive read-out (DRO) operations. On the other hand, non-volatile memories using the ferroelectric-gate field-effect transistor (Fe–FETs) with a metal/ferroelectric/semiconductor gate stack, in which the channel conductivity is controlled by the spontaneous polarization of ferroelectric materials, make non-destructive read-out (NDRO) operation possible. Metal-ferroelectric-semiconductor field-effect transistors (MFS–FETs) with a single transistor (1–*T*) memory cell have promising advantages of high-density integration, NDRO operation, low power consumption, high-speed operation, better endurance and potentially fewer processing steps.[1)–3)] However, MFS–FETs have some problems brought about by the interface reaction between ferroelectric materials and Si substrates. That is, the interdiffusion of constituent elements and the unwanted low dielectric SiO_2 layer is generated at the interface of the ferroelectric film and Si substrate while depositing the ferroelectric thin film on the semiconductor substrate. When a gate voltage is applied to this thin SiO_2, the thin oxide turns a moderate gate voltage into a high electric field. So it causes severe stress and high interface trap charges in the SiO_2. The result might be the degradation of the ferroelectric properties of MFS–FETs.[4),5)] To overcome these problems, Fe–FETs with metal/ferroelectric/insulator/semiconductor gate stack (MFIS–FETs) have been proposed, where the insulator as a buffer layer is inserted between ferroelectric materials and Si substrates.[6)] Most of the insulating buffer layers used in an MFIS–FET structure have a high dielectric constant in the range of 10–50, low leakage current, and good interface characteristics. ZrO_2, HfO_2, $HfAlO_x$ and $LaAlO_3$ are representative insulating buffer layers.[7)–10)]

In this work, we prepared a $LaZrO_x$ (LZO) thin film as a buffer layer and $SrBi_2Ta_2O_9$ (SBT) film as a ferroelectric layer in making MFIS–FET devices. The LZO film has been reported to have a high crystallization temperature and relatively high dielectric constant of ≈20, and considered as being thermally stable in contact with Si.[11)] Also, the SBT film is one of the most promising candidates for a 1–*T* type FeRAM because of its high fatigue endurance, good retention, and low leakage current.[12)]

Finally, we fabricated the n-channel ferroelectric-gate FET with Au/SBT/LZO/Si structure, and then investigated the physical and electrical properties of the fabricated MFIS–FETs.

2. Experimental work

We prepared the $LaZrO_x$ (LZO) solution with a 0.1 M concentration and the $SrBi_2Ta_2O_9$ (SBT) solution with 0.3 M concentration, respectively. Also, a p-type (100) silicon wafer was prepared in making the n-channel MFIS–FET devices. The substrate was dipped in a diluted HF solution to remove the native oxide layer from the surface of Si. The fabrication procedure of devices is briefly shown in **Figure 1**.

At first, the field oxide as a diffusion barrier was formed by the thermal oxidation process. After defining the source and drain region, the phosphosilicate glass (PSG) thin film was spin-coated as a doping source of phosphorus (P). Then the diffusion was performed at 1050°C for 1 min by rapid thermal annealing (RTA). For the deposition of the ferroelectric film and buffer layer, the PSG and diffusion barrier oxide layer was removed from the wafer surface. The LZO thin film as a buffer layer was deposited on Si using the sol–gel method. After the crystallization of a buffer layer, the LZO film was dry-etched by the reac-

† Corresponding author: B.-E. Park; E-mail: pbe@uos.ac.kr

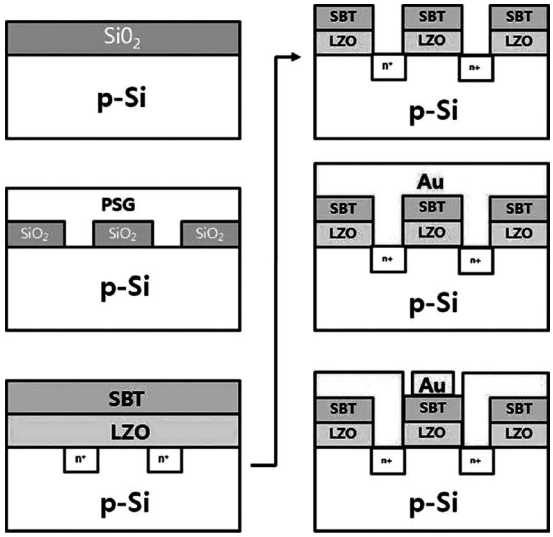

Fig. 1. Fabrication process of Au/SBT/LZO/Si MFIS–FETs.

tive ion etching (RIE) method to open contact holes in the drain and the source region. The SBT film as a ferroelectric layer was then spin-coated on patterned-LZO/Si structures. Prior to the crystallization of a ferroelectric layer, a pre-baked SBT film was wet-etched by soaking it into a BOE to open contact holes. After opening the contact holes, the SBT film was crystallized at 800°C for 30 min in O_2 atmosphere by RTA. The thickness of the LZO buffer layer and SBT film were about 35 nm and 450 nm, respectively. In fact, our previous work revealed that the memory window width increased as the SBT film became thicker in MFIS structure.[13] However, for a thicker SBT film, a partial cracking at the film surface was observed frequently. Thus, we set the film thickness 450 nm in this study. A gold electrode was deposited on the surface of the SBT film using thermal evaporation, and then patterned with gold etchant to define the gate and to make contact with drain and source region. Subsequently, the n-channel ferroelectric-gate FET with Au/SBT/LZO/Si structure was fabricated.

The physical and electrical properties of the fabricated MFIS–FETs were investigated using atomic force microscopy (AFM), X-ray diffraction (XRD) measurements, HP 4280A capacitance-meter and HP 4155C precision semiconductor parameter analyzer, respectively.

3. Results and discussion

Figure 2 shows *C–V* and *J–V* characteristics of the LZO thin film annealed at 750°C. The measurement of the *C–V* characteristics was performed with a ±5 V bias sweep at 1 MHz. As shown in this figure, no hysteresis was observed in the *C–V* curve. No hysteresis particularly meant that there is little chance for a rechargeable oxide trap to exist at the interface between the LZO film and the Si substrate. On the other hand, although the flat band shifted slightly in the negative direction, the extent was negligible. The equivalent oxide thickness (EOT) determined from the accumulation capacitance value was about 17.53 nm. The value of the leakage current density at 5 V was about 1.4×10^{-7} A/cm^2, which indicated that the film provided a good insulating property.

Figure 3 shows the XRD pattern and the surface AFM image of the 450-nm-thick SBT film on the LZO/Si structure. According to the XRD pattern, the film was crystallized in a poly-

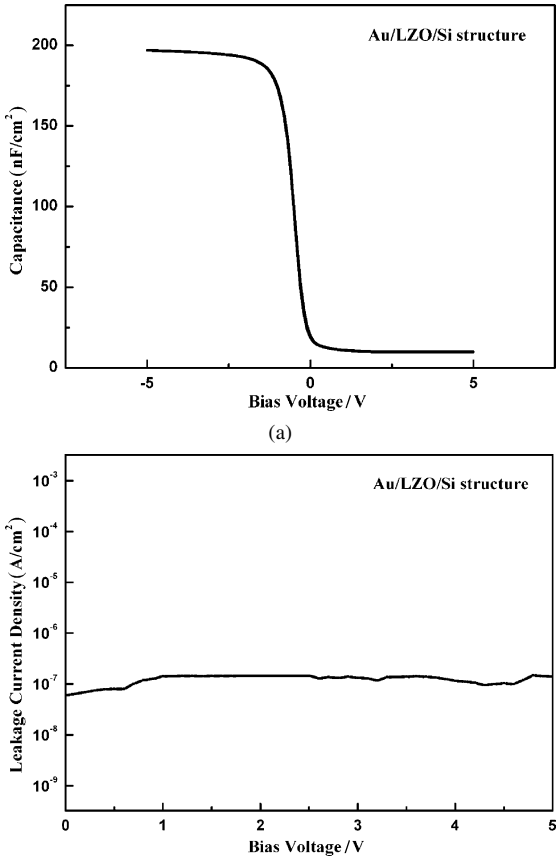

Fig. 2. (a) *C–V* characteristics and (b) the *J–V* characteristics of the 750--annealed LZO thin film on Si.

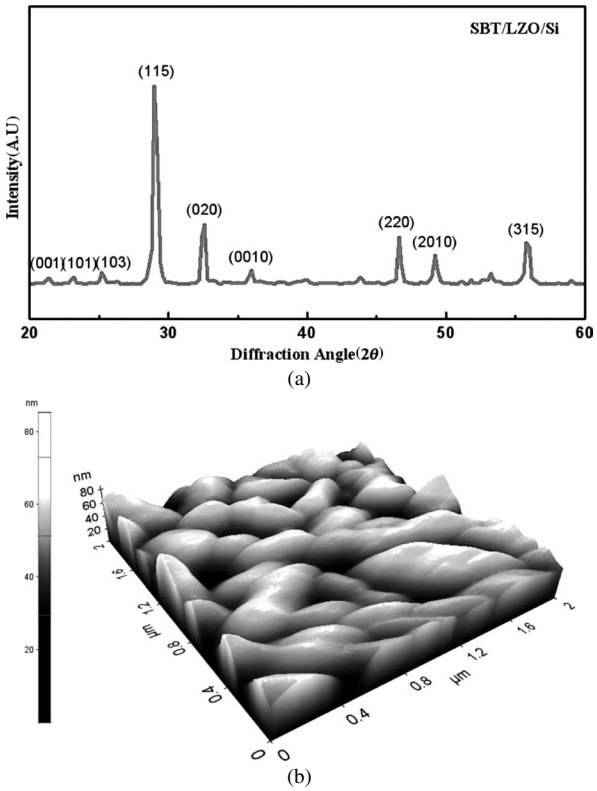

Fig. 3. (a) A typical X-ray diffraction pattern and (b) a surface morphological image of the 450-nm-thick SBT film on LZO/Si structure.

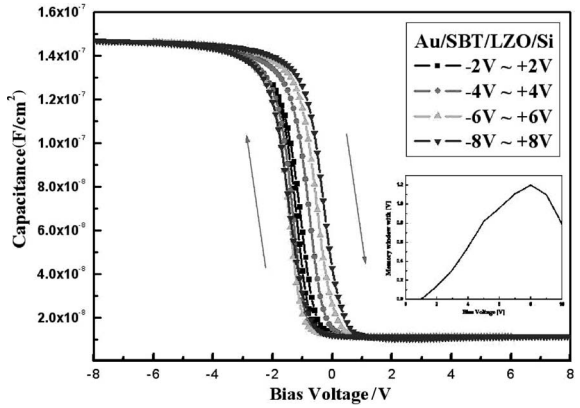

Fig. 4. *C–V* characteristics of the Au/SBT/LZO/Si structure with 450-nm-thick SBT film for a variety of bias sweep voltages.

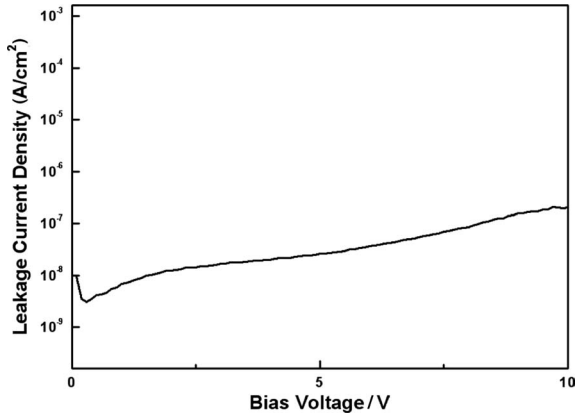

Fig. 5. *J–V* characteristics of the 450-nm-thick SBT on LZO/Si structure.

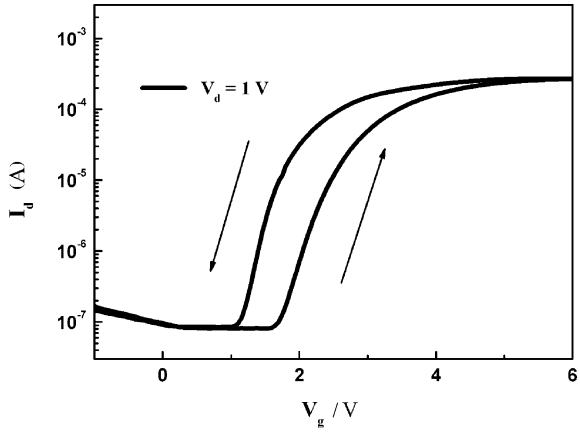

Fig. 6. I_d–V_g curve of MFIS–FETs with Au/SBT/LZO/Si gate stack.

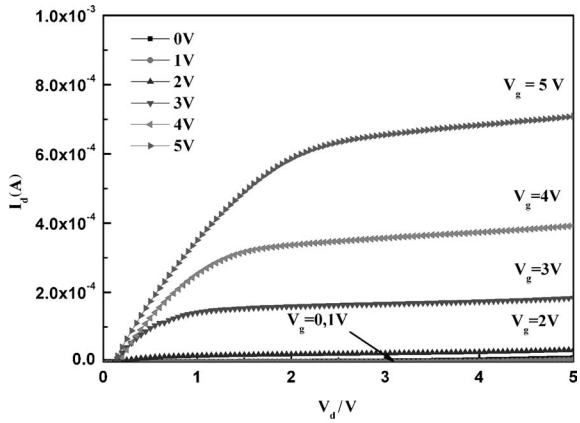

Fig. 7. I_d–V_d curves of MFIS–FETs with Au/SBT/LZO/Si gate stack.

crystalline phase with a highly preferred (115) orientation. In general, film orientation is an important factor for ferroelectric properties, such as polarization, as this is related to direction for dipoles.[14] The low orientation of the main peak causes the problem such as remanent polarization decreasing the characteristic of ferroelectric thin films. The measured area of the surface AFM image was 2×2 μm^2. The average and root-mean-squared (RMS) surface roughness of the 450-nm-thick SBT film were about 8.517 and 11.060 nm, respectively.

Figure 4 shows the *C–V* characteristics of the Au/SBT/LZO/Si structure with 450-nm-thick SBT film for a variety of bias sweep voltages. As shown in the figure, the memory window width increased as the bias sweep voltage increased but began to decrease when the applied sweep voltage exceeded ±8 V. The maximum value of the memory window width was about 1.2 V at a bias sweep voltage of ±8 V. Also, clockwise hysteresis loops were observed, which indicated a switching of the ferroelectric polarization of SBT film.

Figure 5 shows the *J–V* characteristics of the 450-nm-thick SBT on LZO/Si structure at a bias voltage in the range of 0–10 V. The leakage current density was lower than 1×10^{-7} A/cm^2 at 8 V. The measured value of the leakage current density, one of the most important properties for a MFIS structure, showed good characteristics.

Figure 6 shows drain current (I_d) versus gate voltage (V_g) characteristics of the n-channel Fe–FETs with Au/450-nm-thick SBT/LZO/Si structure. To examine the ferroelectric effect, the I_d–V_g curve with a counterclockwise hysteresis loop were logarithmically measured . The applied gate voltage sweep ranged from –1 V to 6 V and the drain voltage was fixed at 1 V. The leakage current density was lower than 1×10^{-6} A/cm^2 and the current on/off ratio was about 10^3. Also, the memory window (threshold shift) width was about 0.7 V due to the ferroelectric nature of the SBT film.

Figure 7 shows the drain current (I_d) versus the drain voltage (V_d) characteristics of the fabricated MFIS–FETs for gate voltages from 0 V to 5 V. The I_d–V_d curve showed typical n-channel MFIS–FETs *C–V* characteristics. The drain current at 5 V applied to the gate was found to be about three orders of magnitude less than the drain current for 0 V applied to the gate in the saturation region.

Fe–FETs with Au/SBT/LZO/Si structure were successfully fabricated and showed relatively good characteristics. However, the memory window width measured from I_d–V_g curve was smaller than the memory window width of Au/SBT/LZO/Si structure in Fig. 4.

4. Conclusions

We have fabricated the n-channel MFIS–FETs with an Au/SBT/LZO/Si structure. The thickness of the LZO buffer layer and the SBT film were about 35 nm and 450 nm, respectively. The LZO film on Si showed no hysteresis loop in the *C–V* curve

and also a good insulating property. The SBT film on LZO/Si structure was crystallized in a polycrystalline phase with a highly preferred (115) orientation and the memory window width increased with the increase of the bias sweep voltage. The I_d–V_d characteristics of the fabricated Fe–FETs showed typical n-channel MFIS–FETs C–V characteristics and the current on/off ratio was about 10^3. Also, the memory window (threshold shift) width was about 0.7 V.

From these results, we have confirmed that the LZO film in the Au/SBT/LZO/Si structure effectively accomplished the role of the insulating buffer layer. Consequently, the MFIS structure with an LZO buffer layer would be suitable for NDRO-type ferroelectric memories with Fe–FETs.

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References

1) J. F. Scott and C. A. Paz de Araujo, *Science*, **246**, 14004 (1989).
2) K. Takahashi, K. Aizawa and H. Ishiwara, *Jpn. J. Appl. Phys*., **45**, 5098 (2006).
3) S. Sinharoy, H. Bobay, D. R. Lampe and M. H. Francombe, *J. Vac. Sci. Techno. A*, **10**, 1554 (1992).
4) Y. Shichi, S. Tanimoto, T. Goto, K. Kuroiwa and Y. Tarui, *Jpn. J. Appl. Phys*., **33**, 5172 (1994).
5) M. Lim, T. S. Kalkur, *Integr. Ferroelectric*, **14**, 247 (1997).
6) B.-E. Park, K. Takahashi and H. Ishiwara, *J. Kor. Phys. Soc*., **46**, 346 (2005).
7) Y.-U. Song, J.-S. Park, J.-W. Yoon, G.-G. Lee, B.-E. Park, C.-J. Kim, Y.-S. Choi and J.-H. Koh, *Integrated Ferroeletrics*, **84**, 203 (2006).
8) B.-E. Park, K. Takahashi and H. Ishiwara, *Appl. Phys. Lett*., **85**, 4448 (2004).
9) B.-E. Park and H. Ishiwara, *J. Kor. Phys. Soc*., **42**, S1149 (2003).
10) M. Takahashi and S. Sakai, *Jpn. J. Appl. Phys*., **44**, L800 (2005).
11) H. Okuyucu, E. Celik, M. K. Ramazanoglu, T. Akin, I. H. Mutlu, W. Sigmund, J. E. Crow and Y. S. Hascicek, *IEEE Trans. Appl. Supercond*., **11**, 2889 (2001).
12) H. S. Choi, E. H. Kim, I. H. Choi, Y. T. Kim, J. H. Choi and J. Y. Lee, *Thin Solid Films*, **388**, 226 (2001).
13) J. H. Im, H. S. Jeon, J. N. Kim, J. H. Kim, G. G. Lee, B. E. Park and C. J. Kim, *Journal of Electroceramics* (Online first).
14) M. Nagata, D. P. Vijay, X. Zhang and S. B. Desu, *Phys. Status Solidi*, **157**, 75 (1996).