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Electrical properties of $Al_2O_3/La_2O_3/Al_2O_3$ films using various tunnel oxide thicknesses for non-volatile memory device applications

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The electrical properties (including memory windows and leakage current densities) of $Al_2O_3/La_2O_3/Al_2O_3$ (ALA) films equipped with 5 nm, 7.5 nm, and 10 nm tunnel oxide layer were investigated. The dielectric constants of all of the tunnel oxide films using Al_2O_3 were the same and the equivalent oxide thickness was dependent on film thickness. The optimized conditions were exhibited in the ALA films with a 5 nm tunnel oxide. The memory window of the ALA films using the 5 nm tunnel oxide was about 1.31 V in the program condition (11 V for 10 ms) and in the erase condition (–13 V for 100 ms). Measurement of the leakage current density showed that all of the films are sufficient for use with flash memory device.

Key-words : SONOS, Memory window, Flash, High-k dielectrics, La_2O_3, MOCVD

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1. Introduction

NAND flash memory has recently become one of the main memory platforms for the next generation in high density semiconductor storage. Its share in memory market has rapidly increased.[1)] However, current NAND flash memory uses a floating gate for charge storage, which has some drawbacks. These disadvantages include a threshold voltage (V_{th}) shift and a wide distribution of V_{th}. Moreover, stress-induced leakage current (SILC) causes problems in scaling down NAND flash memory.[2)] The first mention of scaling problem whithin the flash memory industry was made in the 2002 ITRS roadmap. The 2007 ITRS roadmap revealed that a 30 nm limit on flash memory devices using a floating gate was expected.[3)–4)] Hence, a floating gate can no longer be used for charge storage in non-volatile flash memory.

The concept of a SONOS (silicon–oxide–nitride–oxide–silicon) type memory device was proposed in order to solve these problems. Since the SONOS type device has a stacked structure such as multi-layer films, the floating gate is not necessary. Hence, the SILC is basically prevented and structural problem such as capacitance coupling can be solved.[5)] In addition, the SONOS device offers many advantages, including its applicability to the conventional CMOS process, and its suitability for System on Chip (SoC) applications and for low power operation.[5)] However, this SONOS device has its own set of problems, such as erase speed and retention time. While many studies aimed at solving these problems and putting SONOS devices to commercial use are currently underway, many research groups have recently begun investigation the possibility of using high dielectric (high-k) materials instead of the ONO (oxide–nitride–oxide) structure.[6)–8)] When high-k materials are used as a trap layer, tunnel and blocking oxides can take advantage of decreased program/erase voltage and of improved retention characteristic as compared to the SONOS device. These advantages can lead to superior charge trap characteristics.[9)–10)]

In this study, we investigated the charge trap characteristics of a new structure utilizing the high-k materials instead of the ONO (same as SONOS) structure. We fabricated an Al_2O_3–La_2O_3–Al_2O_3 (ALA) structure. In particular, the memory characteristics using varying thicknesses of tunnel oxide were examined by depositing 5 nm, 7.5 nm, and 10 nm of Al_2O_3 tunnel oxide.

2. Experimental procedure

The $Al_2O_3/La_2O_3/Al_2O_3$ films shown in **Fig. 1** were deposited on (100) n-type Si wafers (SILTRON, Korea) using the MOCVD system. La(tmhd)$_3$ tetraglyme adduct [Tris(2,2,6,6-tetramethyl-3,5-heptanedionato) lanthanum (III) tetraglyme adduct, $La(C_{11}H_{19}O_2)_3{\cdot}CH_3(OCH_2CH_2)_4OCH_3$, Strem Chemical INC., USA] and Al-acetylacetonate [Al(CH_3COCH), Strem Chemical, INC., USA] were used as a precursors for the La and Al metal, respectively. N_2 was used as a carrier gas for the La and Al precursors. Prior to deposition, the wafers were cleaned with organic solvents. They were then treated with a 10% hydrofluoric (HF) solution to remove native oxide.

Amorphous phases of the La_2O_3 and Al_2O_3 films appear at 350°C, and the grain boundary of the crystalline phase can be a path for leaking charge. As a result, we deposited all of the films

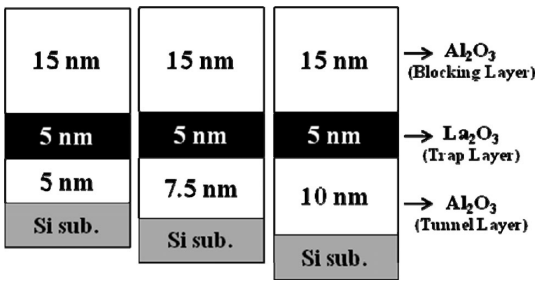

Fig. 1. A schematic diagram of the ALA multi-layered structure with 5 nm, 7.5 nm, and 10 nm tunnel oxide layers deposited on the Si substrate.

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at 350°C to prevent growth of the crystalline phase. Investigation of the substrate temperature of the La_2O_3 and Al_2O_3 films has been described previously.[11)–12)] The substrate temperature was maintained at 350°C during deposition, and the working pressure was maintained at 5 torr (266.6 Pa). The film thickness was measured by an ellipsometer (Gartner, L117, $\lambda = 632.8$ nm). To measure electrical properties of the ALA films, (metal - blocking oxide - trap layer - tunnel oxide – semiconductor) capacitors (Pt/$Al_2O_3/La_2O_3/Al_2O_3$/Si) were fabricated. The Pt electrode of the capacitor was fabricated using magnetron sputtering with shadow masks. The capacitor area was 9.25×10^{-4} cm^2 for all of the specimens. We measured the *I–V* characteristics using HP4145B semiconductor parameter analyzer in order to estimate the leakage current. A *C–V* analysis was performed using a Keithley 590 *C–V* analyzer at 1MHz in order to investigate memory window and the optimized program voltage.

3. Results and discussion

Figure 2 shows the equivalent oxide thickness (EOT) and dielectric constants of 5 nm, 7.5 nm, and 10 nm Al_2O_3 films. According to the 2007 ITRS roadmap, the SiO_2 currently used as a tunnel oxide can not be used in flash memory device in the future since the thinning of the oxide from the scaling down causes a large amount of leakage current density. Hence, high-k materials should be used as tunnel oxide instead of SiO_2. Using these high-k materials offers a few advantages, including a decrease in the amount of leakage current density at the same EOT and a lower powered operation at the same physical thickness. Since Al_2O_3 is well known as a good electrical insulator and the dielectric constant of Al_2O_3 is higher than that of SiO_2, we decided that Al_2O_3 would be an optimum candidate for use as a tunnel oxide instead of SiO_2. In this experiment, the dielectric constant of all of the Al_2O_3 films was about 7.25. The EOTs of the 5 nm, 7.5 nm, and 10 nm Al_2O_3 films were 2.99 nm, 3.98 nm, and 5.14 nm, respectively.

Figure 3 shows the memory windows (ΔV_{th}) of the ALA structures with a tunnel oxide thickness of 5 nm, 7.5 nm, and 10 nm as a function of the program voltage at 1 ms and 10 ms. All of the specimens were measured at the same *C–V* conditions: a double sweep mode from –4V to 4V. In order to approximate the optimum charge trapping conditions, we measured the *C–V* characteristics of all of the specimens from 1 ms to 10 ms using program voltages from 5 V to 13 V. At 5 V and 7 V, the memory windows of all of the specimens were about 0.3 V. The value of these memory windows was too low for application of the flash memory, as there was no charge trapping. On the other hand, charge trapping of the specimens occurred at 9 V and 11V. At these voltages, the memory windows of the ALA film with a 5 nm tunnel oxide were about 0.75 V and 1.7 V, respectively. Those of the ALA film with the 7.5 nm tunnel oxide layer were about 1.1 V and 1 V, respectively. However, the memory window of the ALA films with a 10 nm tunnel oxide was too low value for application in flash memory devices at every program voltage condition. We concluded that there was not enough charge trapping at all of the program conditions, since the 10 nm tunnel oxide layer is relatively thick. Since the *I–V* curve of ALA film showed a breakdown causing leakage at 12.1 V in our previous *I–V* experiment, it can be concluded that the memory windows of the ALA films decrease at program conditions of 13 V.[12)] Hence, we conclude that using ALA films with 5 nm and 7.5 nm tunnel oxide layers provides a suitable structure for charge trapping at program conditions between 9V and 11V.

Since the memory windows of the ALA films equipped with

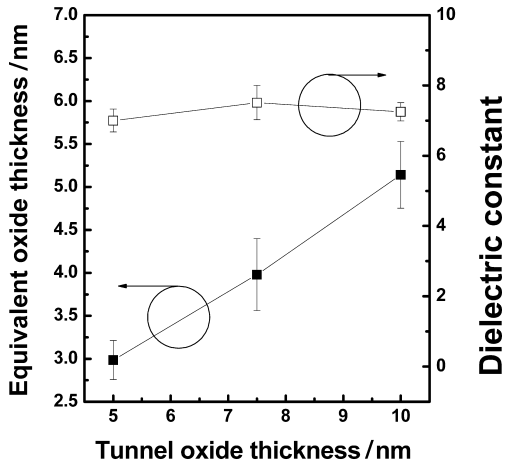

Fig. 2. Equivalent oxide thickness and dielectric constant of 5 nm, 7.5 nm, and 10 nm Al_2O_3 films.

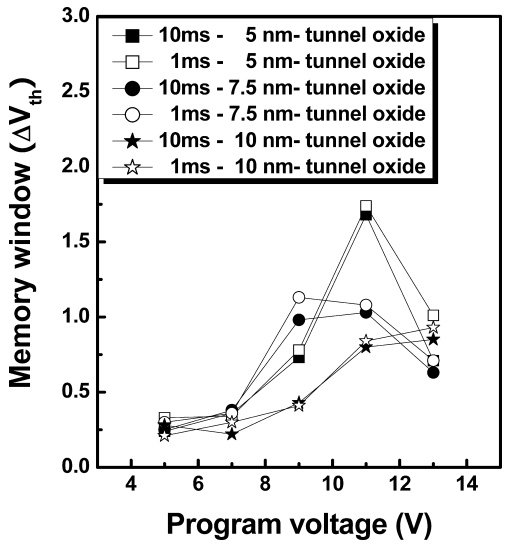

Fig. 3. Memory windows (ΔV_{th}) of the ALA structures equipped with tunnel oxide layer of 5 nm, 7.5 nm, and 10 nm as a function of the program voltage at 1 ms and 10 ms.

the 5 nm tunnel oxide layer was similar to that of the specimens with a 7.5 nm tunnel oxide layer, we concluded that the thinner 5 nm tunnel oxide has advantages over the 7.5 nm tunnel oxide in that it has a lower program/erase voltage and a faster program/erase operation. Hence, ALA films with a 5 nm layer of tunnel oxide were chosen for further study. **Figure 4** shows the fully erased, and then programmed and erased *C–V* curves of the ALA films with a 5 nm tunnel oxide layer. The full erase operation eliminates the charge remaining in the films before the program/erase operation, measured from –11 V to –17 V and from 0.1 sec to 4 s. The best condition for the full erase operation was –15 V for 2 s, and the V_{th} at the best condition was –0.21 V. The measurement at –15 V for 4 sec and at –17 V was almost as good as the best condition. In the program operation, we measured from 5 V to 13 V and from 1 ms (10^{-3} s) to 1000 ms. In the erase operation, we measured from –5 V to –13 V and from 1 ms to 1000 ms. The best condition for the program operation was 11 V for 10 ms, while for the erase operation it was –13 V for 100 ms. The V_{th}s for the program and erase operation were 1.36 V and

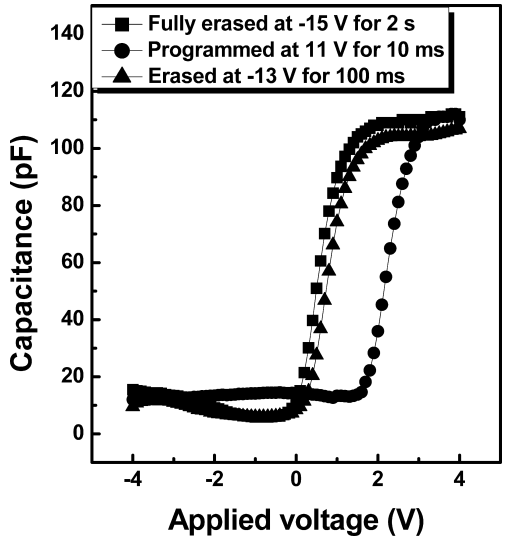

Fig. 4. Fully erased, programmed and erased, *C–V* curves of the ALA structures utilizing the 5 nm tunnel oxide.

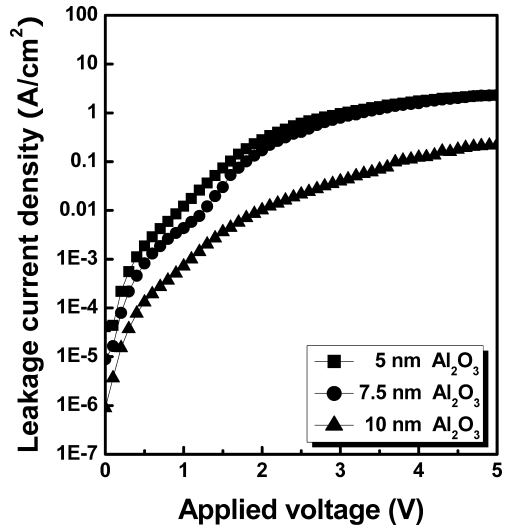

Fig. 5. Leakage current densities of the ALA structures with 5 nm, 7.5 nm, and 10 nm tunnel oxide layers as a function of applied voltage.

0.05 V, respectively. The optimized memory window of the ALA films equipped with a 5 nm tunnel oxide was 1.31 V. Although the difference in the conduction band offset between Al_2O_3 (2.8 eV) and La_2O_3 (2.3 eV) was less than 0.5 eV, the memory characteristic of the ALA structure with a 5 nm tunnel oxide are sufficient for a flash memory device, due in part to recently improved detection limits of sense amplifier.[13)]

Figure 5 shows the leakage current densities of the ALA structures as a function of applied voltage. Although the leakage current of the device can increase up to about 10–12 A/cm^2 or more under instantly applied voltage, the durability of the device holds up well under such conditions. However, this can not be guaranteed in the continuously applied voltage mode, such as the *C–V* or *I–V* sweep mode at high voltage range. Since the operation voltage of the recent device is also below an absolute value of 3 V, the measurement in the high voltage range is meaningless. Hence, we measured the *I–V* characteristics of the ALA films with the three different tunnel oxide thicknesses from 0 V to 5 V in order to investigate the leakage current of the films in the continuously applied voltage mode. The *I–V* characteristics of the films depended on the film thickness. The leakage current density of the ALA films with a 5 nm tunnel oxide at 1 V was 1.21×10^{-2} A/cm^2, the highest value in this experiment. According to the 2007 ITRS roadmap, however, this value is acceptable for flash memory. Since leakage current densities of all of the films were below 10^{-1} A/cm^2 at 1V, which is the range widely used for device operation, we conclude that these films can be used in the flash memory device.

4. Conclusions

In order to investigate the charge trap characteristics of ALA ($Al_2O_3/La_2O_3/Al_2O_3$) films equipped with 5 nm, 7.5 nm, and 10 nm tunnel oxide layers, we deposited a 5 nm La_2O_3 trap layer on these tunnel oxides. Then, a 15 nm Al_2O_3 blocking oxide films was deposited onto the La_2O_3 films. The memory window characteristics of the ALA films equipped with a 5 nm tunnel oxide layer were superior to those of the other films. The optimized program and erase conditions of the ALA structure with the 5 nm tunnel oxide were 11 V for 10 ms and –13 V for 100 ms, respectively. In addition, the *I–V* characteristics of the ALA films depended on film thickness, and all of the achieved values were sufficient for flash memory devices.

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