Simulation for thickness change of PRAM recording layer

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In this study, the phase change behavior of PRAM recording layer during 1 cycle operation was investigated by finite element method (FEM) simulation. The JMAK equation was used for simulation of phase change behavior of the $Ge_2Sb_2Te_5$ (GST) recording layer of PRAM. The RESET simulation of the PRAM unit cell of 100 nm thick recording layer model shows that the amorphous region of the recording layer was partially crystallized after RESET current was removed. This crystallization may cause the sensing error for data reading operation of PRAM. To avoid this sensing error, a 25 nm thick recording layer model of PRAM was subjected to simulation. The thin (25 nm) recording layer model shows higher cooling rate than the thick (100 nm) layer model. Therefore, the crystallization fraction of the thin layer model during RESET operation was decreased and the difference of electrical resistance between RESET and SET state of thin recording layer model was greater than the thick recording layer model.

Key-words : PRAM, Simulation, JMAK, Recording layer, Thickness

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1. Introduction

Phase change random access memory (PRAM) is the device operated by resistance difference between amorphous and crystalline state of recording layer of chalcogenide material.[1),2)] Applied current makes recording layer into amorphous or crystalline state by joule heating. **Figure 1** shows PRAM operation. High current (reset current) makes amorphous mark in recording layer by heating and quenching. This operation is called reset operation. Amorphous mark is banished by low current (set current) heat treatment. This operation is called set operation. Typically, Generation of heat in semiconductor device causes negative effect such as degradation of material. Therefore, excess heat must be removed through heat sink. However, feature of PRAM is using joule heating for writing operation. In PRAM reset operation, low cooling rate increases heating rate of the recording layer. However, insufficient cooling rate during quench process makes reset operation fail by enough time for crystallization of amorphous area. High cooling rate makes amorphous area more easily, but reset operation needs high reset current by loss of heat. Therefore, balancing of cooling rate is important point for PRAM unit cell design.

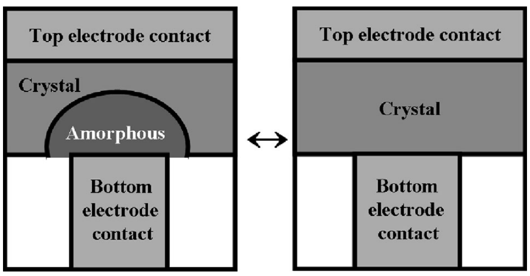

Fig. 1. Basic operation of PRAM.

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2. Simulation model

2.1 The JMAK equation for non-isothermal calculation

In this study, crystallization behavior of recording layer material of PRAM ($Ge_2Sb_2Te_5$, GST) was calculated by following JMAK (Johnson–Mehl–Avrami–Kolmogorov) equation.

$$\chi(t,T) = 1 - \exp\left[-\left(1.07\times10^{21}\times t\times\exp\left(-\frac{2.11\text{eV}}{K_B T}\right)\right)^{2.5}\right]$$

Where, χ means the crystalline volume fraction, t is the heat treatment time, T is the temperature and K_B is the Boltzmann's constant. Frequency factor of 1.07×10^{21}, Avrami's constant of 2.5 and activation energy of 2.11 eV were used in this study. Basically, the JMAK equation was designed for isothermal heat treatment;[3)–6)] however, operation of PRAM is a non-isothermal process. To apply the JMAK equation to non-isothermal process simulation modeling, it is assumed that the temperature is constant in a unit increment. Therefore, the crystalline volume fraction was calculated from the current temperature and summation of current increment time and the time which was calculated back from JMAK equation using crystalline volume fraction of previous increment. **Figure 2** shows the crystallization volume fraction calculated by above method during quenching the recording layer material (GST). As shown in Fig. 2, the calculated result indicates that the crystallization rate increases with decreasing cooling rate. This result reflects the real crystallization phenomenon. Also, this result is comparable with reported quenching rate value[7)] (10^{11} °C/min) for obtaining amorphous GST. Therefore, it can be concluded that the JMAK equation can be applicable to simulation of non-isothermal process for PRAM.

2.2 The modeling

The commercial finite element method program ABAQUS/standard 6.6–1 was used for simulation. Unit cell structure proposed by one of the authors was used for analysis with modification.[8] **Figure 3** shows 100 nm and 25 nm recording layer models of PRAM structure analyzed in this study. Reset and set currents were supplied from tungsten bottom electrode. Outside boundary temperature of the model was maintained at 25°C. The modeling for 100 nm recording layer was consisted of 20 ns heating, 200 ns cooling with quenching, and cell resistance reading steps. The modeling for 25 nm recording layer was consisted of 20 ns heating, 200 ns cooling with quenching, cell resistance reading and second heating (set process) for 15 ns. The material properties used for simulation are given in **Table 1**. **Figure 4** shows the sheet resistance (from which electrical conductivity can be obtained) and crystalline volume fraction of GST according to temperature. Figure 4 was obtained by in-situ reflectivity method[7] and ex-situ 4-point probe measurement. The recording layer material was assumed to have the crystalline phase in the initial condition. Reset current was supplied by 5.1–5.6 mA for 100 nm layer model and 7.1–7.5 mA for 25 nm layer model during 20 ns. Set current was 6.3–6.5 mA for 25 nm model during 15 ns.

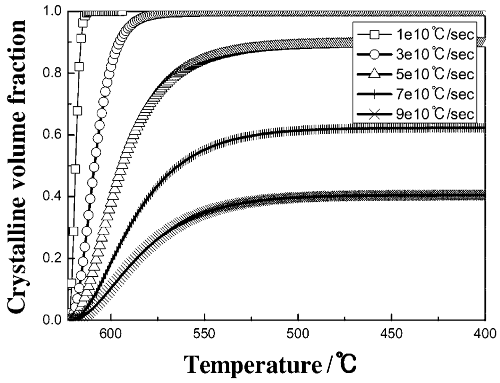

Fig. 2. Calculated crystalline volume fraction along the temperature during quenching.

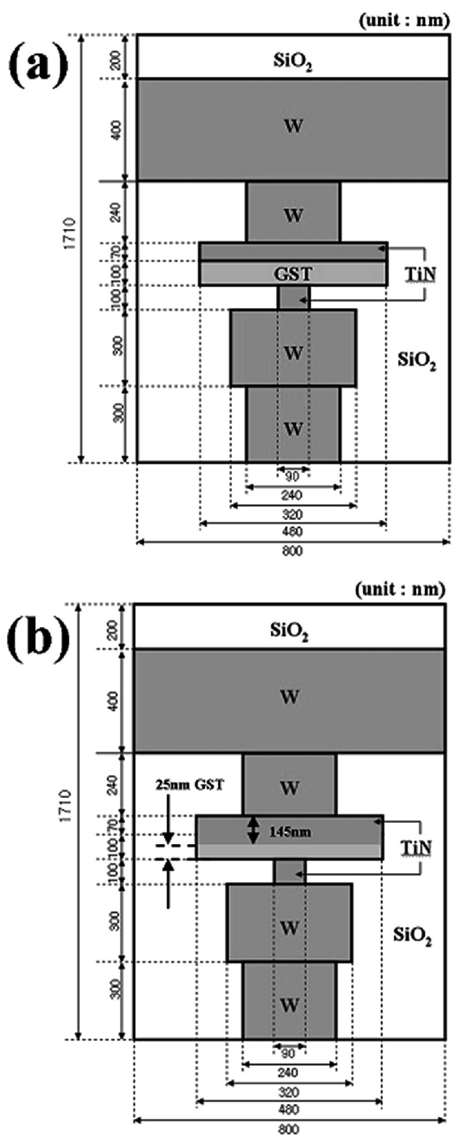

Fig. 3. Models for simulation; (a) 100 nm recording layer model, (b) 25 nm recording layer model.

Table 1. Material Properties Used for Simulation

$Ge_2Sb_2Te_5$	Density	6.2 g/cm^3 (crystalline)
		5.8 g/cm^3 (amorphous)
	Melting point	623°C
	Thermal conductivity	0.018 J/(mKs) (crystalline)
		0.003 J/(mKs) (amorphous)
	specific heat	1.93 J/(cm^3/K)
	Electrical conductivity	Ref. Fig. 4
W	Density	19.3 g/cm^3
	Thermal conductivity	1.78 J/(mKs)
	specific heat	2.58 J/(cm^3/K)
	Electrical conductivity	1.75×10^7/Ωm
SiO_2	Density	2.33 g/cm^3
	Thermal conductivity	0.014 J/(mKs)
	specific heat	3.1 J/(cm^3/K)
	Electrical conductivity	1.0 × 10–14/Ωm
TiN	Density	5.4 g/cm^3
	Thermal conductivity	0.13 J/(mKs)
	specific heat	3.235 J/(cm^3/K)
	Electrical conductivity	1.0×10^6/Ωm

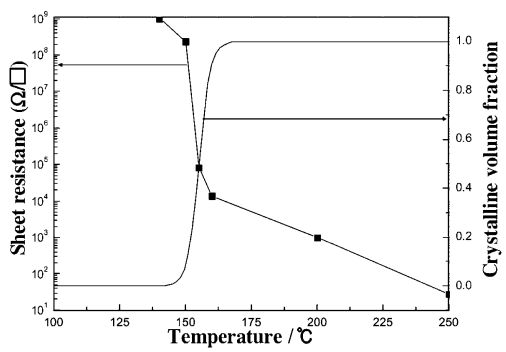

Fig. 4. Variation of sheet resistance and crystalline volume fraction of $Ge_2Sb_2Te_5$ as a function temperature.

3. Result and discussion

3.1 Reset operation result for 100 nm recording layer model

Figure 5 shows the simulation results of amorphous area distribution in recording layer after 20 ns heating and after 200 ns cooling for 100 nm recording layer model. As shown in Fig. 5, all reset current results have the hemisphere shapes of amorphous areas after the reset current was applied for 20 ns. However, after 200 ns cooling, all of the amorphous area distribution results show partial crystallization. Especially, the largest amorphous area was observed after 5.6 mA of the reset current was applied; however, the amorphous area was mostly crystallized during cooling process. Reasons of these phenomena are assumed as followings. While amorphous area neighboring with TiN bottom electrode contact remained amorphous itself, the upper area of amorphous hemisphere which occurred in 20 ns result was mostly changed to crystalline. This is because thermal conductivity of GST recording layer material was ten times lower than that of TiN bottom contact material. The heat generated under side of the recording layer is considered to pass through the TiN bottom contact but the heat generated at upper or center of the recording layer is considered to pass through GST material that has poorer thermal conductivity than TiN. Therefore, cooling rate of the upper or the center of the amorphous in the recording layer was lower than the amorphous area of the under position neighboring with TiN bottom electrode contact. **Figure 6** shows the maximum temperature of the recording layer and the ratio of resistance of initial state to reset state according to the reset current. As shown in Fig. 6, it can be understood that the largest resistance ratio was obtained at 5.4 mA. Above 5.5 mA reset current, it is considered that quite much electric energy was used to recrystallize the amorphous phase compared with 5.4 mA reset current was supplied. The best resistance ratio 5.94 was obtained at 5.4 mA. However, this is not sufficient for smooth reading operation in real device that needs resistance ratio at least higher than 10. These results mean that 100 nm recoding layer model has insufficient cooling rate for formation of amorphous mark. To solve this problem of crystallization of amorphous area, cooling rate of the recording layer must be increased by modifying the PRAM unit cell structure model.

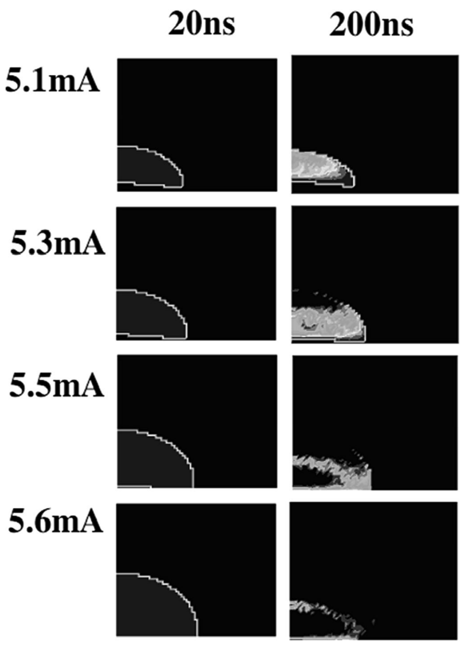

Fig. 5. Amorphous area distributions in recording layer after 20 ns reset current applied and after 200 ns cooling.

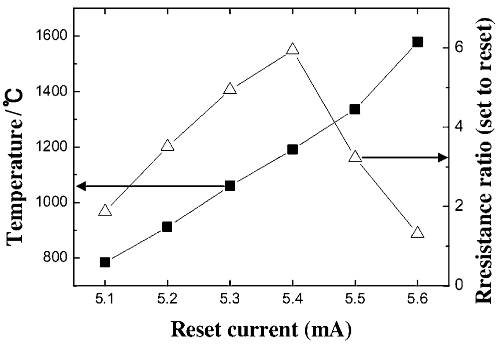

Fig. 6. Maximum temperature of the recording layer and the ratio of the resistance of initial state to reset state according to the reset current.

3.2 Reset operation result of 25 nm recording layer model

By the simulation result for 100 nm recording layer model, it was confirmed that an amorphous area neighboring with TiN bottom contact remained as amorphous state after cooling step due to the good thermal conductivity of TiN. Therefore, it is expected that if the generated heat can pass through TiN upper electrode contact, it is possible to obtain greater cooling rate for entire recording layer. The thinner 25 nm recording layer model was designed to decrease the distance from the amorphous area to the upper TiN electrode. In this model, reset current was increased above 7 mA because 25 nm recording layer model has larger heat loss than 100 nm recording layer model. **Figure 7** shows the amorphous area after heating-cooling process for 25 nm model. **Figure 8** shows the maximum temperature of the recording layer and the ratio of resistance of initial state to reset state according to the reset current for 25 nm model. As shown in Fig. 7, a little crystallization occurred at the center of the amorphous area but the entire amorphous area remained for all currents. As can be seen in Fig. 8, the ratios of resistance of initial state to reset state are proportional to the reset current in 25 nm model. Also, it can be seen in Fig. 8 that the reset currents above 7.3 mA give sufficient resistance ratio for smooth reading operation in real device. From these results, it is concluded that the 25 nm model has higher potential to show normal operation in real device than 100 nm model because 25 nm model has sufficient cooling rate. However, heat loss is a severe problem for 25 nm model compared with 100 nm model. Therefore, it is con-

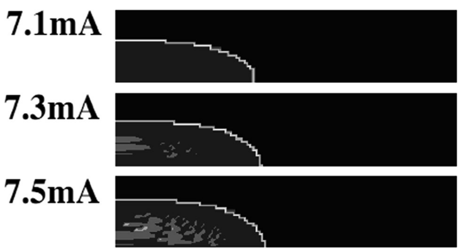

Fig. 7. Amorphous area distributions in recording layer after 200 ns cooling for 25 nm model.

cluded that thickness of the recording layer should be decided between 25 nm to 100 nm.

3.3 Set operation result for 25 nm recording layer model

To evaluate set operation, the reset current of 7.3 mA was chosen for 25 nm recording layer model, because this condition showed the appropriate ratio of resistance of initial state to reset state for reading operation and 7.3 mA is relatively small reset current. Set current was 6.3–6.5 mA for 15 ns. **Figure 9** shows amorphous area distribution in the recording layer after the set current was applied for 15 ns. As shown in Fig. 9, all set current conditions show entire crystallization after 15 ns. This set time is similar to a previous report.[7] Set operation is basically crystallization process; therefore, set operation needs higher temperatures than the crystallization temperature and sufficient time. It is expected that normal set operation will be easily performed even at lower set current than 6.3 mA.

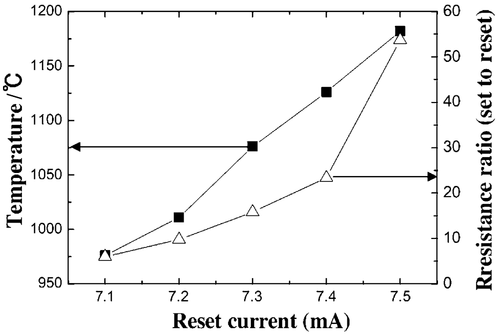

Fig. 8. Maximum temperature of the recording layer and the ratio of the resistance of initial state to reset state according to reset current for 25 nm model.

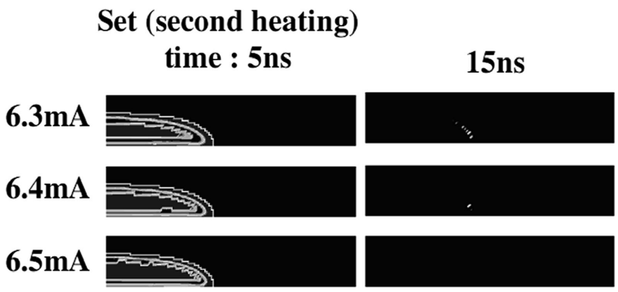

Fig. 9. Amorphous area distribution in recording layer after according to set currents were applied for 15 ns.

4. Conclusions

The simulation method was used to evaluate operation of PRAM unit cell. Crystallization behavior of GST recording layer of PRAM was calculated by JMAK equation. Reset operation of PRAM was seriously affected by unit cell structure and cooling rate. Thick recording layer was found to cause crystallization in amorphous area by quenching during reset operation due to the poor cooling rate. To avoid this problem, the recording layer should be between 25 and 100 nm. However, too thinner recording layer may cause higher reset current. Therefore, the cooling rate and the reset current must be balanced when PRAM unit cell is designed.

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